4 + 1-transistor pixel architecture for high-speed, high-resolution CMOS image sensors

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A pixel architecture is introduced which allows a drastic reduction of the column capacitance of a monolithic pixel array. It consists of a classic 4T pixel architecture together with an extra switch added at regular positions in the column array and shared by a group of pixels of the column. In this way, each pixel will see an output capacitance proportional to the number of pixels sharing the extra switch and the total number of extra switches.

Introduction: The use of CMOS technologies in image sensing has speeded-up the development of high frame rate image sensors. Compared to traditional CCD technology, CMOS imagers have an increased parallelism and can integrate on-chip processing elements such as column-level analogue to-digital converters (ADCs), high-speed digital drivers etc. Imagers capable of a high frame rate are required in an increasing number of applications such as robotics, bio-medicine, security etc. High frame rates simplify the image processing algorithms and can trade time resolution for spatial resolution [1].

In monolithic CMOS pinned-photodiode (PPD) large resolution arrays, there are three main factors limiting the frame rate:

- pixel access time
- A-to-D conversion time
- digital I/O speed.

The pixel access time is limited by the capacitance of the row select line and also the capacitance of the column bus, which is proportional to the number of pixels per column. In this Letter we focus on the reduction of the column bus capacitance.

As seen in Fig. 1, the column bus is shared by all the pixels in one column. The capacitance on the column line is dominated by the source diffusion of the select switches (C_{sw}) [2]. Increasing the speed is possible by increasing the current biasing of the source follower in the pixels driving the column bus. However, this would obviously lead to higher power consumption, possibly larger voltage drops along the supply lines and a lower output voltage swing of the pixel source followers owing to the increased gate–source voltage needed to conduct more current.

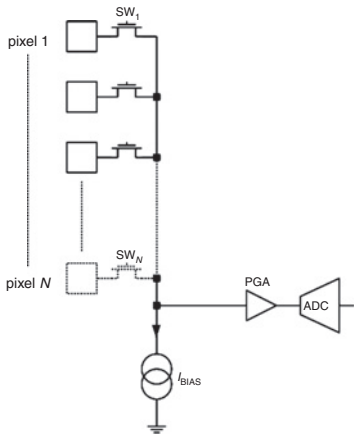

Fig. 1 *Row select switches sharing column bus in common monolithic pixel array*

To decrease the bus capacitance, more buses could be placed in parallel. For instance, two buses would halve the capacitance seen by the pixels of the same column. However, this requires additional control signals and could increase the pixel pitch and increase the complexity of the routing in the layout. Another method used in high-speed imaging is the addition of buffers at regular positions, e.g. at a distance equal to the square root of the number of pixels in the column, by replacing the pixel in that position [2]. The missing pixel information is reconstructed by interpolating neighbouring pixels in the same manner as in the case of defective pixels. But this means that the number of defective pixels increases considerably, requiring extra image processing power.

In this Letter we propose a pixel architecture composed of a classic 4T pixel (but the technique can be applied to a 3T pixel as well) and an extra switch as shown in Fig. 2. The extra switches are placed at a distance equal to the square root of the number of pixels in the column. To maintain pixel uniformity, dummy switches are used in the remaining pixels; however, they are not connected to the signal lines to avoid their contributing to the total output capacitance.

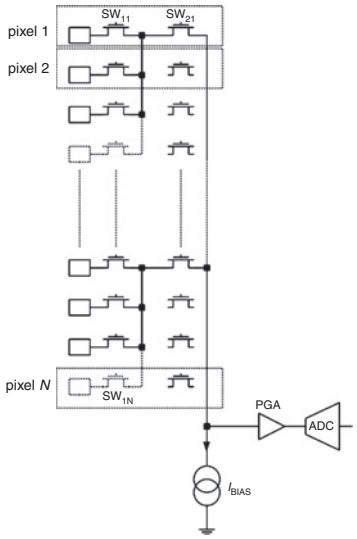

Fig. 2 *Proposed method with second switch inserted at regular positions*

The total capacitance given by the source diffusion of the select switches in each column is reduced from NC_{sw} in the conventional architecture to $2\sqrt{N}C_{SW}$ in our case, where N is the number of pixels in the column and C_{sw} is the single-switch capacitance. For instance, the column of an ultra-high-definition TV (UHDTV) format array composed of 4320 pixels would have a column capacitance reduction of approximately 32 times. The second switch adds a series resistance to the signal path, which could reduce the pixel signal swing. However, given the reduction of the capacitance, lower column currents are needed. By using lower currents also the voltage drop of the first switch and the gate to source voltage of the source follower is lowered, improving the dynamic range of the sensor. Careful sizing of the source follower should be used, however, in order to avoid an increase of the thermal noise when lower biasing currents are used. The disadvantage of the proposed architecture is the increased pixel pitch owing to the addition of a second pixel select switch (can be minimum size transistor), a second row control line and a second signal bus line. The row control signal of the additional switch can easily be generated with shift registers. The number of shift registers needed is only $\sqrt{N}$ and also the power consumption is only a fraction of that required to control the first switch of the pixels.

Simulation results: Two UHDTV column arrays comprising 4320 pixels and double readout circuitry (top and bottom, hence 2160 pixels per column line) have been simulated including the parasitic devices extracted from the layout. A 0.18 μm CMOS technology was used. Simulation results were obtained using Cadence Spectre. One column applies the proposed readout method while the other consists of a conventional 4T pixel readout. Both columns use the same 10 μA current bias for the pixel source followers. The voltage on the column bus is shown in Fig. 3. Although the capacitance of the source diffusion of the select switches is reduced by approximately 23 times, other parasitic capacitances such as the signal bus capacitance and the current bias capacitance remain constant. The simulated settling time of the output of the proposed pixel architecture is 20 ns, instead of 300 ns for the conventional one. To provide 240 frames/s required by UHDTV, the pixel readout including the analogue-to-digital conversion (ADC) must be performed within 1.9 μs. A column ADC can convert in 0.5 μs [3]. The correlated double sampling can be performed in the analogue domain [3] with one A-to-D conversion per pixel. Owing to the reduced pixel output settling time, the reset noise and signal can be read out in 40 ns instead of 600 ns. A sufficient time budget of more

than 1.3 μs (instead of 0.8 μs) is thus available to perform the reset of the floating diffusion (FD) node and the charge transfer from the photodiode to the FD [4].

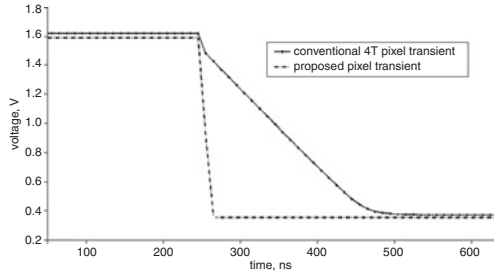

Fig. 3 *Settling time simulation of UHDTV column array format comparing classic 4T pixel architecture with proposed 4T + 1 architecture*
Shift in voltage amplitude is due to extra switch resistance

Conclusions: A method has been proposed to decrease the column capacitance of a pixel array by half of the root square of the number of pixels of the column. The effectiveness of the method has been simulated for a UHDTV column array, showing an output settling time reduction of approximately 15 times.

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